Zero Ripple Single Stage AC-DC LED Driver with Unity Power Factor

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***Abstract*—The single stage LED Driver can achieve relatively high efficiency, however the low frequency ripple current is too significant if high power factor has been achieved. With two stages AC-DC LED Driver structure, we can achieve high power factor and tight current regulation at the same time. However, the drawback of the two stage structure is relatively low efficiency and high component cost. In this paper, an innovative single stage LED Driver with ripple cancellation technology has been proposed. We can achieve almost as high efficiency and low component cost as single stage LED Driver while maintaining comparable performance to the two stages LED Driver. Our experimental prototype can achieve 1.5mA Pk-Pk 120Hz ripple current, 0.99 power factor and 85.5% efficiency for a universal AC input, 35W (50V-0.7A) output application.**

I. INTRODUCTION

Due to high luminous efficiency and long lifespan of LEDs, LED lighting fixtures are becoming a more and more popular choice in general. For different lighting applications, the key design consideration for the LED Driver shifts a lot. Designers need to make trade-offs between cost, space, efficiency, and design complexity in order to make an overall optimization for a particular application. In this paper, we will discuss design issues with median power level, 30W-50W, AC-DC LED Driver with electrical isolation requirement.

In order to achieve higher efficiency, low component cost and increase power density, several single stage LED Drive solutions have been proposed in [1-9]. Due to safety concern, isolation is needed between AC line and LED string. There are cases when the LED Driver terminal are exposed to the external environment or LED string are accessible during usage, making isolation necessary. The single stage flyback LED Driver can be a very good topology candidate for our discussed application. The overall component cost for the single stage flyback LED Driver is quite low while good power factor and decent efficiency can be achieved. However, the common issue for single stage LED Driver is usually excessive low frequency ripple current from LED Driver output, which is independent of topology. There is always an instantaneous input and output power difference that exists in a half line cycle. The energy difference in a half line cycle is buffered by output capacitor. A low frequency voltage ripple then present on LED Driver output capacitor due to the charge and discharge action in every half line cycle. Because of the low internal impedance characteristic of the LED load, this significant ripple voltage produces a significant in phase LED ripple current as well. This low frequency LED ripple current will be represented as flicker in the light output. Individual may or may not be able to directly sense lighting flicker at double the main frequency, which is depended on the susceptibility of that individuals. However scientific data has shown that people can resolve flicker at frequency between 100Hz to 150Hz. Even subject is not aware of the flicker, some symptoms, such as malaise, headaches, and visual impairment developed.

A easy fix to alleviate the excessive ripple current is to increase bulky electrolytic storage output capacitors at LED Driver output. However these capacitors take a lot of PCB space, increase the total volume and significantly increase the component cost. An alternative solutions to reduce the ripple current while also keeping a small amount of output capacitance have been proposed in [10-12]. Solution in [10] is to make design trade-offs between achieving high power factor and the required output storage capacitance. By injecting input harmonics, the LED ripple current has been greatly reduced. However, at the same time, this solution greatly scarifies the power factor and increases harmonic current level. In order to keep high power factor, input current need to be shaped to follow input voltage which is the root cause of power imbalance between input and output during a half line cycle. The active power storage solution has been proposed in [11-12] to accommodate the instantaneous power difference without bulky output capacitor. Figure 1 shows the concept of this solution. A Bi-directional DC-DC converter is connected in parallel with LED load as an active energy storage device. When input power is higher than output power, the Bi-directional converter will absorb the excessive input power and store it in capacitor C_{aux} .When input power is less than output power, the energy previously stored in C_{aux} will be transferred back to output.

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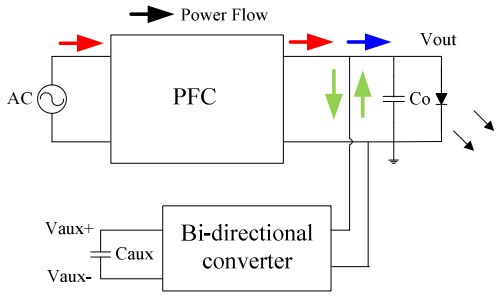


Fig. 1 LED Driver with active energy storage

This active energy storage solution can achieve high power factor, low output capacitance requirement while minimizing the low frequency LED ripple current at the same time. However, there are also drawbacks from this solution.

1. A significant amount of output power has been converted first by PFC then back and forth by the Bi-directional converter before it is finally delivered to the output. The theoretical efficiency of this solution will have an obvious drop from a conventional single stage solution.

2. The peak voltage across capacitor C_{aux} can be relatively high as ceramic capacitor is used in [11-12]. This high voltage imposes significant voltage stress on the power devices of the Bi-directional converter. High voltage rating device is needed. The component cost from the Bi-directional converter make this solution less desirable.

A conventional two stages LED Driver can achieve high power factor and tight output current regulation at the same time. The topologies for front stage PFC and second stage DC-DC can vary depended on the application. Figure 2 shows a popular two stages AC-DC LED Driver structure with power rating around 30W-50W.

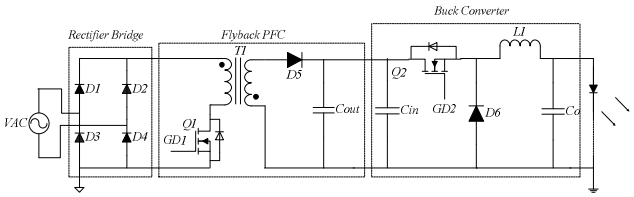


Fig. 2 Conventional two stage flyback PFC plus Buck Converter structure

The front stage flyback converter can achieve high power factor and produce a low intermediate voltage, which can reduce the voltage stress for the second stage DC-DC converter. The second stage buck converter can achieve tight LED current regulation with low component cost and high efficiency. For power level higher than 50W, the front stage PFC topology is gradually shifted from flyback to boost, and the second stage DC-DC changes accordingly too. The choice of topologies is usually made according to the key requirement of that particular product. For example, when the power rating higher than 150W, the first stage PFC is usually built with boost converter in order to minimize component stress and achieve high power factor, while the second stage DC-DC is built with resonant converter for high efficiency. This structure is not a good choice for low to median power level applications in which cost reduction is a great concern. Different power driver topologies have been investigated in [13-17] suitable for different applications. For two stages structure, all output power need to be converted twice, so in general the efficiency is greatly suffered. In addition, a higher component cost and larger PCB board area needs to be paid for two stages structure compare to single stage structure.

A summary of the pros and cons of the above discussed LED Driver solutions is made below:

- Single stage LED Driver can achieve high efficiency and low component cost. However the LED ripple current is too significant if high power factor need to be achieved.

- The solution proposed in [11-12] can greatly reduce the LED ripple current. However, there is a large amount of power being converted three times before it is finally delivered to output. The component cost and design complexity from the Bi-directional converter also make this solution less desirable.

- Two stages LED Driver is a time proofed standard technology. High power factor and tight current regulation can be achieved. Efficiency of the two stages structure is lower than single stage structure in general. A Boost PFC cascaded with a resonant isolated converter can achieve high efficiency, however the component cost is relatively too high for low power application.

The target improvement we are going to make in our proposed solution is to achieve high efficiency, low component cost as the single stage LED Driver while maintaining comparable performance to the two stages solution. Figure 3 illustrates the concept of our proposed solution.

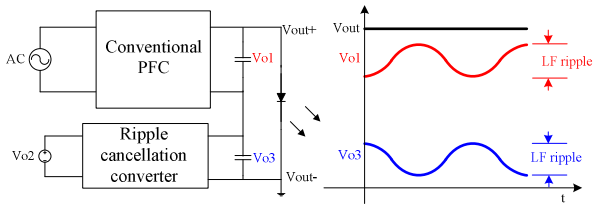


Fig. 3 The concept of our proposed solution

As it is shown in Fig. 3, the output voltage of PFC, $\boldsymbol{V_{o1}}$, is connected in series with the ripple cancellation converter (RCC) output voltage $\boldsymbol{V_{o3}}$. The sum of $\boldsymbol{V_{o1}}$ and $\boldsymbol{V_{o3}}$, $\boldsymbol{V_{out}}$, becomes the voltage across LED string. There are two key features in this solution:

1. $\boldsymbol{V_{o1}}$ has much higher average voltage than $\boldsymbol{V_{o3}}$, so most of the power delivered to the output is directly from PFC converter.

2. The output voltage of the RCC, $\boldsymbol{V_{o3}}$, contains a low frequency AC component which can fully cancel the low frequency output voltage ripple from PFC output $\boldsymbol{V_{o1}}$. This way, the sum of these two voltages is a low frequency ripple free DC voltage and so the LED Driver current is a DC value.

In our experimental prototype, the average output voltage for $\boldsymbol{V_{o1}}$ is 45V and the average output voltage of $\boldsymbol{V_{o3}}$ is 5V. So 90% of the output power is directly transferred from PFC converter while 10% of the output power is transferred from voltage source $\boldsymbol{V_{o2}}$. The voltage source $\boldsymbol{V_{o2}}$ is actually an auxiliary output from the PFC, so only 10% of the total output power has been converted twice. The total efficiency is very close to the single stage LED Driver. Due to a low level of power, voltage and current handled by the RCC, the cost of power components from the RCC is also very low. Very encouraging efficiency, performance and low component cost have been achieved in our experimental prototype.

This paper is organized in the following order: in section II, the operating principle of the proposed technology will be discussed. Section III will review the design considerations. In section IV, the control diagram will be presented with a detailed description. The circuit implementation will be discussed in section V, followed by the experimental result in section VI and the paper ends in section VII with the conclusion.

II. OPERATING PRINCIPLE

Figure 4 shows the power stage structure of the proposed ripple cancellation LED Driver. The input voltage for the RCC is V_{o2} , which is an auxiliary output voltage from the flyback PFC. The RCC is implemented by buck converter for achieving high efficiency and low component cost. The output of the RCC, V_{o3}, is connected in series with the flyback PFC main output voltage, V_{o1}, to provide power to the LED string.

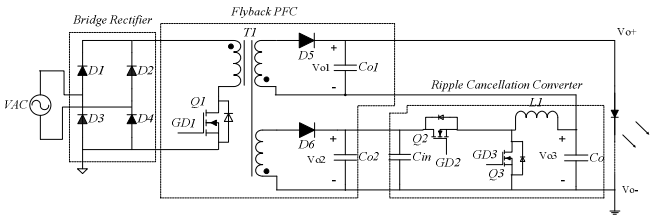


Fig. 4 The proposed ripple cancellation LED Driver

When high power factor has been achieved, a significant ripple voltage at twice the AC line frequency presents itself on the PFC output. The PFC main output, V_{o1}, can be described by Eq. (1) below:

$$V_{o1} = V_{dc1} + V_{rip1} \tag{1}$$

The output of the RCC, V_{o3}, can be described by Eq. (2):

$$V_{o3} = V_{dc3} + V_{rip3} \tag{2}$$

The sum of V_{o1} and V_{o3} becomes:

$$\begin{aligned} V_{out} &= V_{o1} + V_{o3} \\ &= (V_{dc1} + V_{dc3}) + (V_{rip1} + V_{rip3}) \end{aligned} \tag{3}$$

In the above Eqs. (1), (2) & (3), V_{dc1}, V_{dc3} and $(V_{dc1} + V_{dc3})$ represent the DC component of V_{o1}, V_{o3} and V_{out} respectively while V_{rip1}, V_{rip3} and $(V_{rip1} + V_{rip3})$ represent their low frequency AC ripple component respectively. The objective of our proposed ripple cancellation technology is to produce a voltage across the LED string free of low frequency ripple. So that the ripple voltage, V_{rip3}, is produced as a mirrored V_{rip1} by the RCC. We have Eq. (4):

$$V_{rip3} = -V_{rip1} \tag{4}$$

This way, the low frequency ripple component of V_{out}, $(V_{rip1} + V_{rip3})$, becomes zero. Thus, only the DC voltage, $(V_{dc1} + V_{dc3})$, across the LED string and the DC LED current can be obtained.

III. DESIGN CONSIDERATIONS

A. Flyback PFC design consideration

Carefully choosing between current conduction mode for the flyback PFC around 35W power rating is critical to achieve an overall optimization. For the flyback PFC, working at DCM mode with constant on time control can achieve very high power factor and low switching loss. However the current stress imposing on MOSFET and diode is quite high. Working under CCM can minimize the current stress on MOSFET and diode. However, the switching loss become quite high since both turn on and turn off are hard switching. In order to make an overall optimization, we have the flyback PFC working under CRM mode. Low switching loss, reasonable current stress and high power factor can be achieved.

B. RCC design consideration

As we can easily learn from Fig. 4, the output power delivered by V_{o1} has only been converted once by the flyback PFC while the output power delivered by the RCC has been converted twice, firstly by the flyback PFC and then by RCC. In order to achieve high efficiency, we need to reduce the amount of power that has been delivered by the RCC. Since the PFC output, V_{o1}, and the RCC output, V_{o3}, are connected in series, the ratio of the output power they delivering is determined by their averaged voltage ratio. The lower averaged voltage produced by V_{o3}, the less output power delivered by the RCC and the higher overall efficiency we can achieve. In order to minimize the averaged power delivered by the RCC, the DC component of the RCC output voltage, V_{dc3}, is desired to be set as low as possible. However, there is another constraint that has to be met: the minimum output voltage of the RCC has to be above zero since the RCC is implemented by a buck converter. The minimum output voltage produced by the RCC is:

$$V_{o3(min)} = V_{dc3} - \frac{1}{2}V_{rip3(pp)} \tag{5}$$

In Eq. (5), $V_{rip3(pp)}$ represents the peak to peak value of V_{rip3}. The condition of $V_{o3(min)} > 0$ needs to be met when considering the minimum value for V_{dc3}. The AC ripple value of the PFC output is determined by the output power and the output storage capacitance. In our experimental prototype, the AC ripple component V_{rip1} and V_{rip3} are as high as 6V pk-pk. The RCC output is designed to be averaged at 5V DC so that the swing of V_{o3} is in the range of 2V~8V. On the other hand, the peak value of the RCC output sets the minimum input voltage allowed for the RCC converter. The maximum output voltage from the RCC is:

$$V_{o3(max)} = V_{dc3} + \frac{1}{2}V_{rip(pp)} \quad (6)$$

Since the RCC is implemented by a buck converter, the RCC input voltage, V_{o2}, has to be higher than its output voltage. In our experimental prototype, $V_{o3(max)}$ is 8V. V_{o2} is set to be higher than 8V to meet the requirement of $V_{o2} > V_{o3(max)}$.

IV. CONTROL STRATEGY

Figure 5 shows the control diagram of the proposed zero ripple technology. The sum of voltage V_{o1} and V_{o3}, V_o , is the voltage across LED strings. LED current is sensed and compared with the current reference I_{ref} . The error current information is compensated and fed back to primary side controller through opto-coupler. This way, the output voltage V_{o1} can be controlled and the LED current is regulated equal to current reference. The DC voltage of V_{o3} is a fixed value and is set by voltage V_{dc}. V_{dc} is designed according to the analysis covered in Section III. The low frequency ripple voltage of V_{o1} is sensed. V_{dc} subtracting V_{rip1} results V_{ref}, which is the reference voltage for the RCC. This way, the AC component of V_{ref} is a mirrored value of V_{o1}'s low frequency voltage ripple. In order to achieve very good reference tracking, a fast feedback loop for RCC has been designed to allow RCC output voltage, V_{o3}, to closely follow V_{ref}. So the AC ripple component from V_{o1} and V_{o3} cancel each other out very well. A DC voltage appears across the LED string and produces a DC LED current.

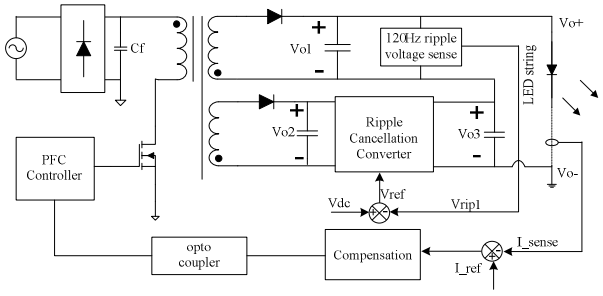


Fig. 5 The control diagram of proposed zero ripple technology

V. CIRCUIT IMPLEMENTATION

In order to cancel low frequency ripple from the flyback PFC output Vo1, a proper designed ripple sensing and conditioning circuit becomes very critical. Figure 6 shows the detailed circuit implementation. From practical points of view, all resistors used for signal conditioning are selected to be within 0.5% tolerance in order to precisely set the AC ripple amplitude. The OpAmps used in AC ripple sensing and conditioning circuit deal with 120Hz frequency signal, so a general purpose low power consumption OpAmp should be good enough. TLV274CDR from TI is chosen in order to lower component cost and static power consumption.

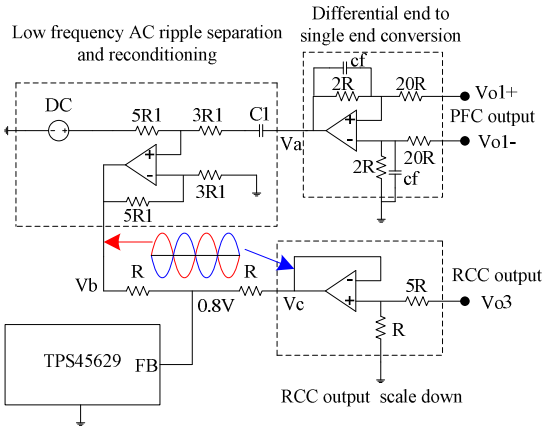


Fig. 6 The circuit implementation of low frequency ripple sensing and conditioning circuit

Since the negative end of the flyback PFC output, V_{o1-}, is connected to the positive end of the RCC output, the voltage ($V_{o1}+$, $V_{o1}-$) is a differential signal pair with respect to controller ground. A differential to single end conversion circuit is built to sense V_{o1}.The voltage V_a is a scale down version of V_{o1} with reference being the controller ground:

$$V_a = \frac{1}{10}(V_{dc1} + V_{rip1}) \quad (7)$$

The high frequency switching noise and ripple presenting on V_a will be filtered by filter capacitor C_f.The DC component of V_a will be blocked by capacitor C1. C1 and R1 is carefully selected to let the low frequency AC ripple fully pass. The low frequency AC component of V_a, $\frac{1}{10}V_{rip1}$, then be amplified by factor $\frac{5}{3}$ and added with a pre-designed DC biasing. The output of this part circuit, V_b, can be described:

$$V_b = 0.8 + \frac{1}{6}.V_{rip1} \quad (8)$$

The average of V_b and V_c will be fed to the feedback pin of buck regulator TPS45629. With a sound feedback design, the FB pin is regulated at 0.8V so we can have:

$$\frac{V_b + V_c}{2} = 0.8 \quad (9)$$

and V_c equals to :

$$V_c = 0.8 - \frac{1}{6}.V_{rip1} \quad (10)$$

Since V_c is also equals to the 1/6 of Vo3, so the output of RCC become:

$$V_{o3} = 4.8 - V_{rip1} \quad (11)$$

As we can obtain from Eq. (11), the low frequency AC ripple from PFC output V_{o1} is mirrored by AC component of V_{o3}, and they will cancel out each other by connecting V_{o1} and V_{o3} in series. The voltage across the LED string becomes a low frequency ripple free DC voltage.

VI. EXPERIMENTAL RESULTS

A low frequency ripple cancellation LED Driver based on a flyback PFC plus RCC structure has been built and tested. Figure 7 shows the key waveform from our experimental prototype. The 120Hz ripple voltage from the flyback PFC output has been mirrored by RCC output. They cancel out each other very well. The sum of these two voltages becomes a DC voltage and a DC LED current has been obtained.

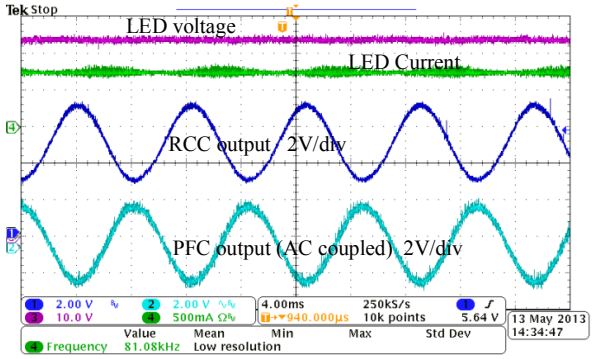
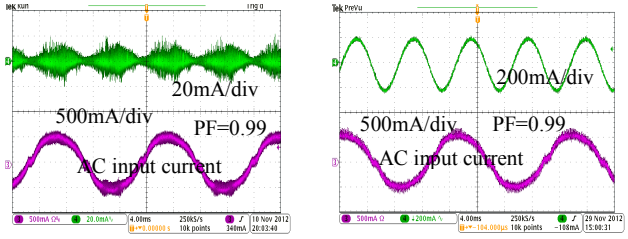


Fig. 7 Ripple cancellation between PFC output and RCC output

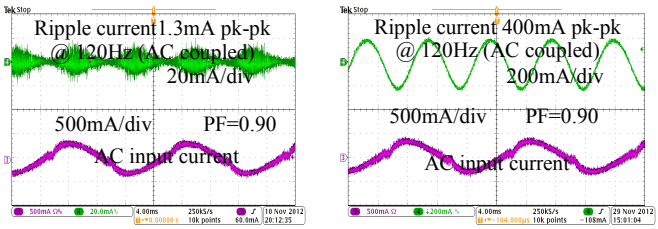
Figure 8 & 9 shows the performance comparison between our proposed ripple cancellation technology and the conventional single stage LED Driver.



(a) (b)

Fig. 8 LED ripple current under 110VAC input: (a) proposed technology; (b) conventional single stage LED Driver.

Both prototypes use the same output capacitor value of 470uF. The LED string used in our experimental setup is made of 23 piece LEDs (part number: LR W5AM-HZJZ-1-Z) connected in series. It has been demonstrated from the waveforms that the 120Hz LED ripple current has been reduced from 400mA Pk-Pk to 1.3mA Pk-Pk with our proposed ripple cancellation technology.



(a) (b)

Fig. 9 LED ripple current under 220VAC input: (a) proposed technology; (b) conventional single stage LED Driver.

The ripple reduction ratio is as great as 266 times. With this new technology, we are able to achieve comparable performance as two stages LED Driver. The digital scope's FFT function is used to measure the amplitude of the 120Hz ripple current, separating it from the high frequency switching ripple current.

Unlike a two stage LED Driver structure where all output power has been converted by both the power stages, 90% of the output power has only been converted once in our proposed technology. So the efficiency of our proposed technology is very close to the efficiency of a conventional single stage LED Driver. The full load efficiency comparison between the conventional single stage LED Driver, the conventional two stages LED Driver as well as our proposed solution has been shown at Fig. 10. With our proposed technology, the efficiency at full load is 85.5%, which is very close to 86.5% efficiency achieved by the single stage LED Driver and is much higher than the conventional two stages solution with 82.5% efficiency.

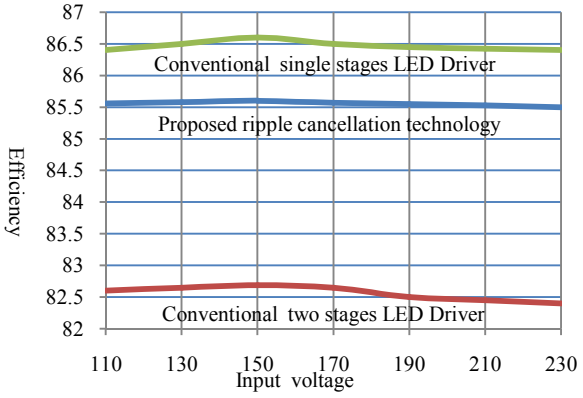


Fig. 10 Full load efficiency comparison between the conventional single stage LED Driver, the conventional two stages LED Driver and our proposed technology

Since only 10% of output power (3.5W, 5V-0.7A) is delivered by the RCC, the level of power processed by the RCC is quite low. Due to the low input and output voltage interface of the RCC, the semiconductor power components of the RCC can be selected with low voltage, low current rating. So the component cost from the RCC is much lower than the secondary stages DC-DC converter in the conventional two stages LED Driver or the Bi-directional

DC-DC in [11-12]. The component comparison made between the RCC and the second stage DC-DC in conventional two stages LED Driver has been shown in Table 1.

TABLE 1. BOM comparison

Components	Second stages DC/DC	RCC
Buck MOSFET	Discrete MOSFET with up to 100V rating	Use a 12V input, 2A output integrated Buck converter (MOSFET, Driver and controller in one package), such as FAN2013, LM2651, TPS54620
Buck diode	Discrete diode with up to 100V rating	
Buck high side Driver	FA5650 high side and low side Driver	
Buck PWM controller	Generic PWM controller	
Buck inductor	RCP1317NP-470MMT, 47uH, 69mohm, 13.5mm diameter, 17.5mm (high)	IHLP2020CZER4R7M11. 4.7uH, 54mohm, 5.2mm x 5.5mm x 3mm (high)
Buck output capacitor	470uF, 63V	20uF / 10V ceramic

The second stage DC-DC converter in the conventional two stages LED Driver needs to handle all the output power. The input voltage is in the range of 60~70V when 50V output voltage is required. We need to use discrete power components because of this voltage rating. On the other hand, due to the low power, voltage and current handled by the RCC, we can use an integrated regulator which includes MOSFETs, gate Driver, and controller. Our proposed solution will be much more cost effective and easy to implement. The output filter inductor and capacitor used in the RCC is also much less expensive than the components used in the second stage DC-DC converter due to lower power handed by them. The overall component cost of our proposed technology is much lower than conventional two stages LED Driver.

VII. CONCLUSION

Due to only a small fraction of output power being handed by the RCC, the efficiency and overall component cost of our proposed technology is very close to single stage LED Driver. An efficiency of 85.5% has been achieved in our 35W, 50V-0.7A prototype. With our proposed ripple cancellation technology, the low frequency LED ripple current has been greatly removed in our experimental prototype. The LED current regulation of our prototype is just as good as the two stage counterpart. No compromise needs to be made between achieving high power factor and the amount of energy storage capacitance used. Near unity power factor and as low as 1.3mA pk-pk 120Hz ripple current have been recorded in our prototype. From practical point of view, another great merit of our proposed structure is the independence operation between power Driver circuit of the RCC and the flyback PFC. The RCC can be designed as a standard module to work with any other PFC as long as the interface has been specified. This feature will further bring down the cost of RCC converter.

REFERENCE

[1] J. Zhang, H. Zeng and T. Jiang, "A Primary-Side Control Scheme for High-Power-Factor LED Driver With TRIAC Dimming Capability," IEEE Transactions on Power Electronics, vol.27, no.11, 2012, pp.4619-4629

[2] X.G. Xie, J. Wang, C. Zhao, Q. Lu and S. Liu, "A Novel Output Current Estimation and Regulation Circuit for Primary Side Controlled High Power Factor Single-Stage Flyback LED Driver", IEEE Transactions on Power Electronics, vol.27, no.11, 2012, pp.4602-4612.

[3] H.H Chou, Y.S Hwang and J.J Chen, "An Adaptive Output Current Estimation Circuit for a Primary-Side Controlled LED Driver," IEEE Transactions on Power Electronics, vol.28, no.10, Oct. 2013, pp.4811,4819

[4] J.T Hwang, M.S Jung, D.H Kim, J.H Lee, M.H Jung and J.H Shin, "Off-the-Line Primary Side Regulation LED Lamp Driver With Single-Stage PFC and TRIAC Dimming Using LED Forward Voltage and Duty Variation Tracking Control," IEEE Journal of Solid-State Circuits, vol.47, no.12, Dec. 2012, pp.3081,3094

[5] S.J. Cheng, Y.C. Yan, C.C. Chuang, H.J. Chiu, Y.K. Lo and S.C. Mou, "A single-stage high efficiency high power factor LED Driver" IEEE Vehicle Power and Propulsion Conference, (VPPC) , 2009, pp.1416-1420.

[6] M. Ali, M. Orabi, M.E. Ahmed, and A.E. Aroudi, "A single stage SEPIC PFC converter for LED street lighting applications" 2010 IEEE International Conference on Power and Energy (PECon), 2010, pp.501-506.

[7] C.A. Cheng, F.L. Yang, C.W. Ku and C.H. Yen, "A novel single-stage high power LEDs Driver," IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE), 2011, pp.2733-2740

[8] Y.Q. Hu, L. Huber and M.M Jovanović, "Single-Stage, Universal-Input AC/DC LED Driver With Current-Controlled Variable PFC Boost Inductor" IEEE Transactions on Power Electronics, vol.27, no.3, 2012, pp.1579-1588.

[9] Y. Li, and C. Chen, "A Novel Primary-Side-Regulation (PSR) Scheme for Single-Stage High-Power-Factor AC-to-DC LED Driving Circuit," IEEE Transactions on Industrial Electronics, vol.PP, no.99, pp.1.

[10] X.B. Ruan, B.B. Wang, K. Yao, S. Wang, "Optimum Injected Current Harmonics to Minimize Peak-to-Average Ratio of LED Current for Electrolytic Capacitor-Less AC–DC Drivers" IEEE Transactions on Power Electronics, vol.26, no.7, 2011, pp.1820-1825.

[11] S. Wang, X.B. Ruan, K. Yao, S.C. Tan, Y. Yang and Z.H Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver" IEEE Transactions on Power Electronics, vol.27, no.11, 2012, pp.4540-4548.

[12] Q.C. Hu and R. Zane, "Minimizing Required Energy Storage in Off-Line LED Drivers Based on Series-Input Converter Modules" ,IEEE Transactions on Power Electronics, vol.26, no.10, 2011 pp.2887-2895.

[13] H.B. Ma, J.S Lai, Q.Y Feng, W.S Yu, C. Zheng and Z. Zhao, "A Novel Valley-Fill SEPIC-Derived Power Supply Without Electrolytic Capacitor for LED Lighting Application," IEEE Transactions on Power Electronics, vol.27, no.6, June 2012, pp.3057,3071

[14] M. Arias, D.G. Lamar, F.F. Linera, D. Balocco, A.A. Diallo and J. Sebastián, "Design of a Soft-Switching Asymmetrical Half-Bridge Converter as Second Stage of an LED Driver for Street Lighting Application" IEEE Transactions on Power Electronics, vol.27, no.3, 2012, pp.1608-1621.

[15] V.D.B. Heinz, S. Georg and W. Matthias, "Power Driver topologies and control schemes for LEDs," Annual Twenty Second IEEE Applied Power Electronics Conference, (APEC), 2007, pp.1319-1325.

[16] Y. Chen, X.K. Wu, Z.M. Qian and W.P. Zhang, "Design and optimization of a wide output voltage range LED Driver based on

LLC resonant topology" IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE), 2011, pp.2831-2837.

[17] R. Dayal and L. Parsa, "Non-isolated topologies for high step-down offline LED Driver applications," Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2012 pp.988-993.

[18] Characterizing and Minimizing LED Flicker in Lighting Applications By Steven Keeping, Electronic Products

[19] Supertex design note "Isolated LED Driver Using the HV9910B "DN-H01